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FIG.1

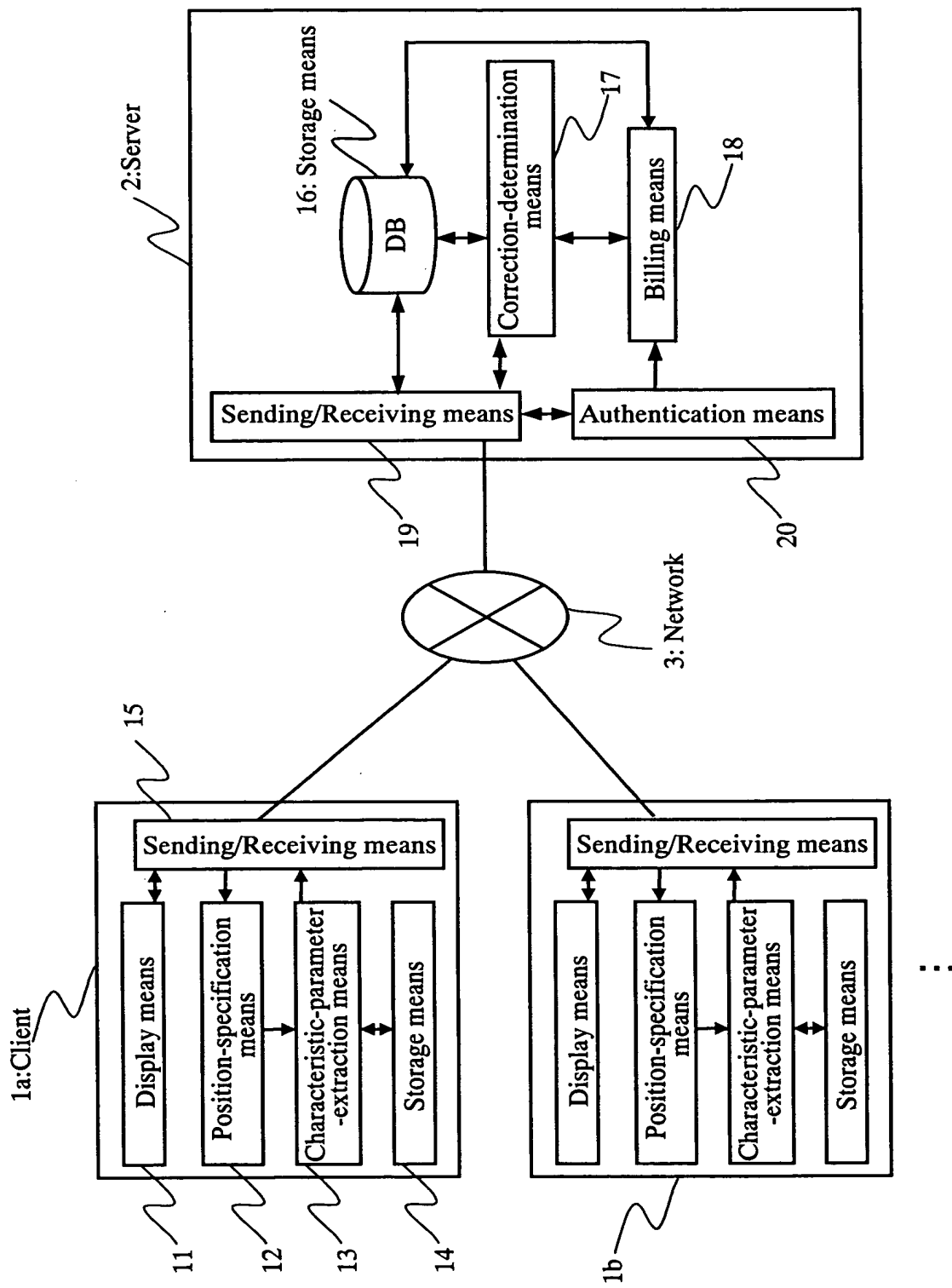


FIG.2

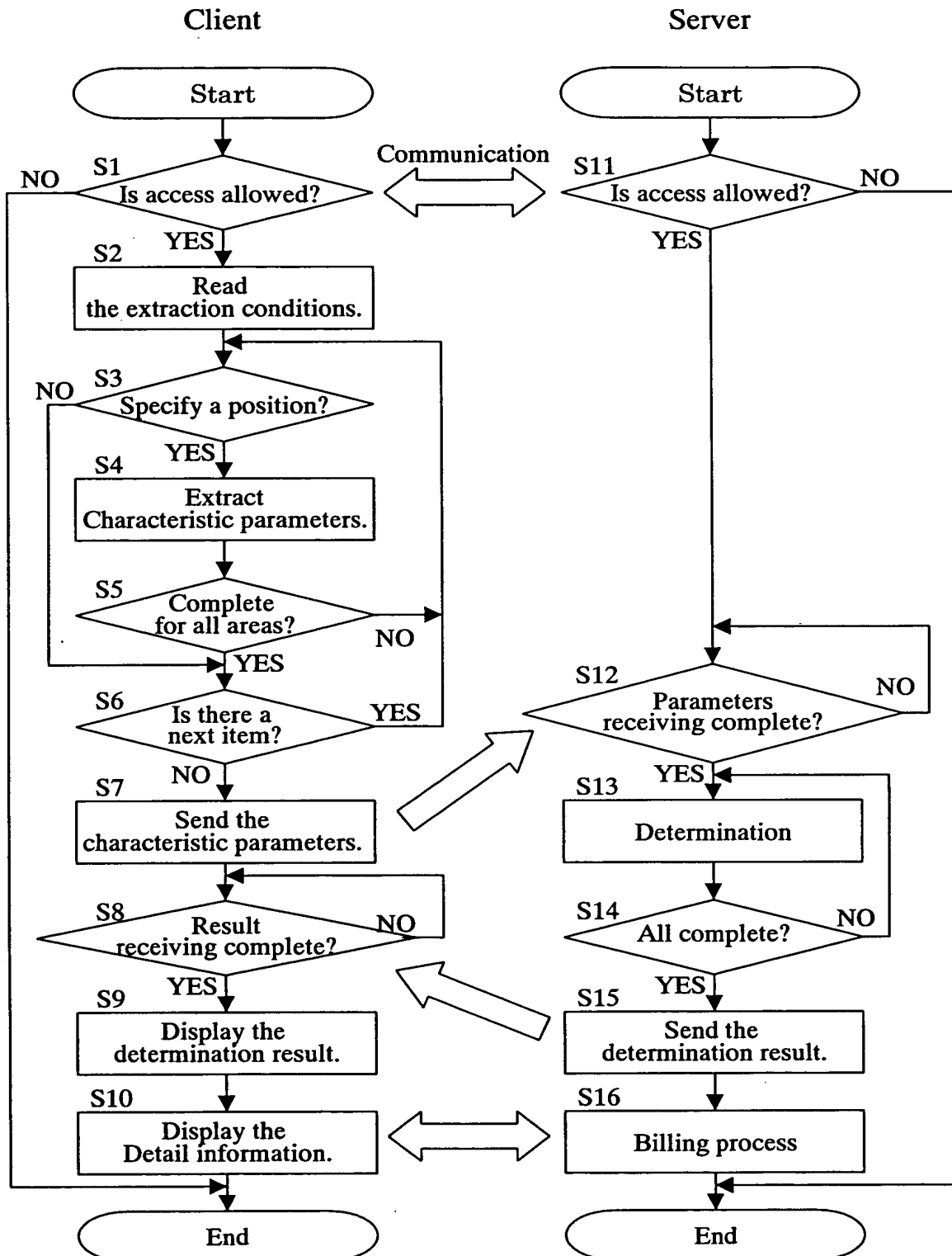


FIG.3

31: Item numbers      32: Position-specification conditions      33: Characteristic-parameter items

Item number	Position-specification conditions	Characteristic-parameter items
1	Slits in the ground plane Signal line extends across the slit.	Frequency of the signal transmitted along the signal line Amount of current flowing in the signal line Area of the plane formed by the signal line and the return-current path
2	LSI Via hole connected to the power-supply plane Bypass capacitor Power-supply line	Coordinates of the LSI power-supply pins Coordinates of the power-supply lines Coordinates of the bypass capacitors Coordinates of the via holes connected to the power-supply plane
3	Signal line formed on the top plane on the edge of the circuit board	Distance between the edge of the circuit board and the signal line Layer on which a signal line is located Maximum frequency of the signal transmitted in the signal line Circuit-board layer construction
4	Ground plane Power-supply plane	Circuit-board layer construction Coordinates of the power-supply plane Coordinates of the ground plane
⋮	⋮	⋮

### 34: Correction-determination standards

Item numbers	Correction-determination standards
1	The amount of radiated noise calculated from the characteristic parameters exceeds the upper limit.
2	There is not bypass capacitor on the power-supply line between the via hole and LSI power-supply pin.
3	A signal line that transmits a signal having a maximum frequency that is greater than a specified frequency is located within a specified distance from the edge of the circuit board.
4	The edges of the power-supply plane are not on the inside within a specified width with respect to the edges of the ground plane.
⋮	⋮

FIG.5

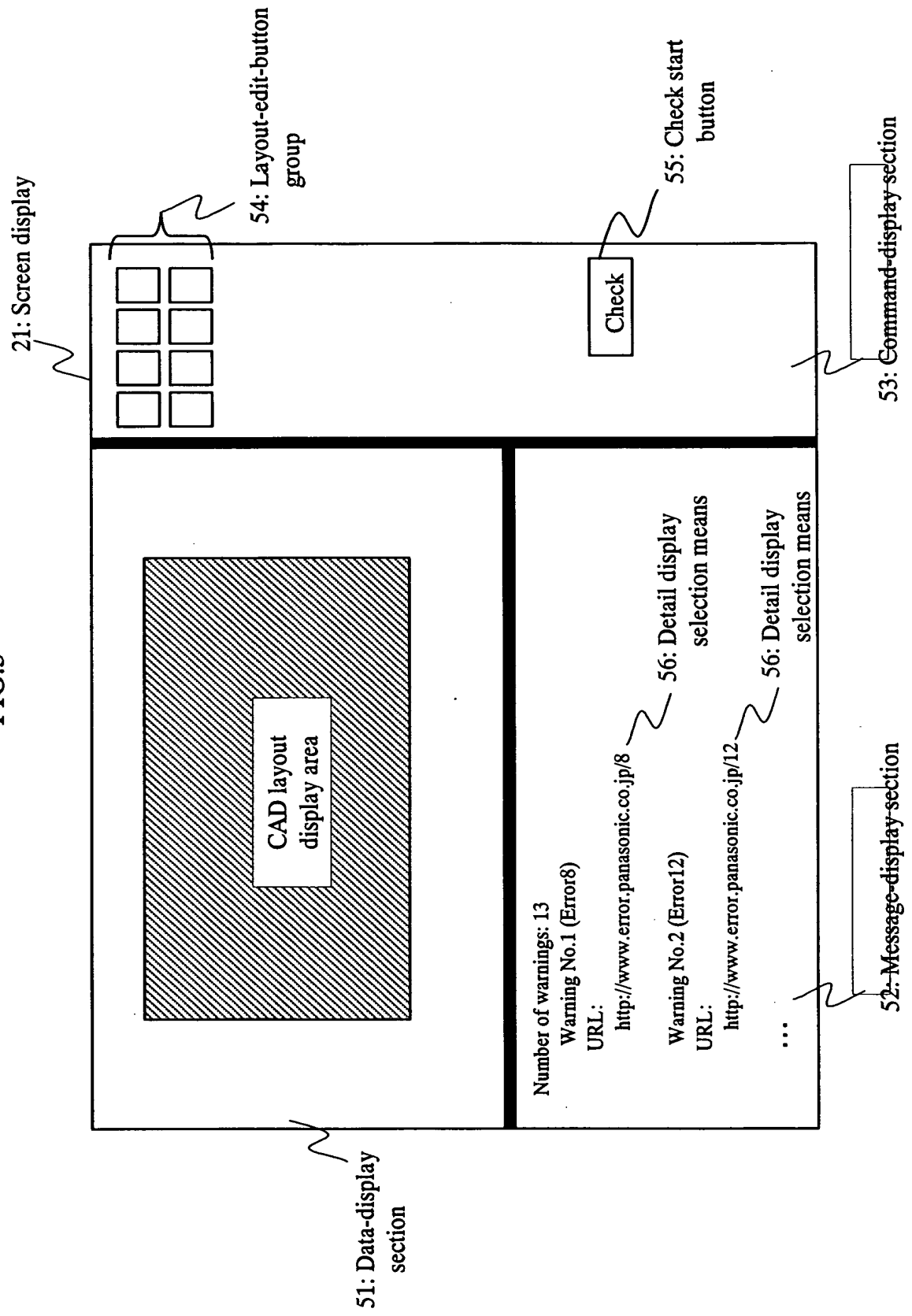


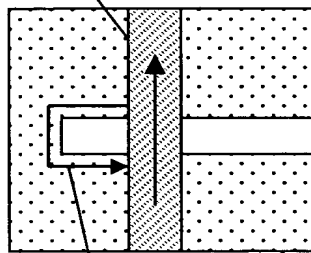
FIG.6

22:Web page

#### 1.4 Basic EMI Plan for a PCB Layout (Line Pattern)

[3] Perform layout such that the return-current path is maintained.

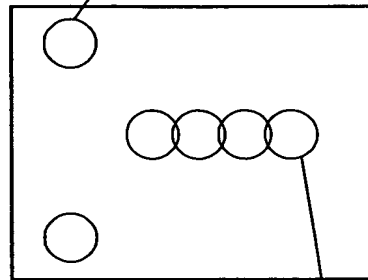
Signal line(First layer)



Return-current path  
(long compared with  
the path of the signal line)

Ground layer  
(Second layer)

Via hole



Occurs when a plurality of via holes  
are made close to each other.

Error 12: Detail information

Coordinates (23.825, 121.25)

There is the possibility of an increase of radiated noise.

Cause: There is a high-speed signal line located  
on a slit, and the return-current path is long.

Correction method:

- (1) Remove the slit under the signal line.
- (2) Add a guard (ground) pattern above the slit.
- (3) Make the layout of the signal line follow the path of the return-current.

FIG.7

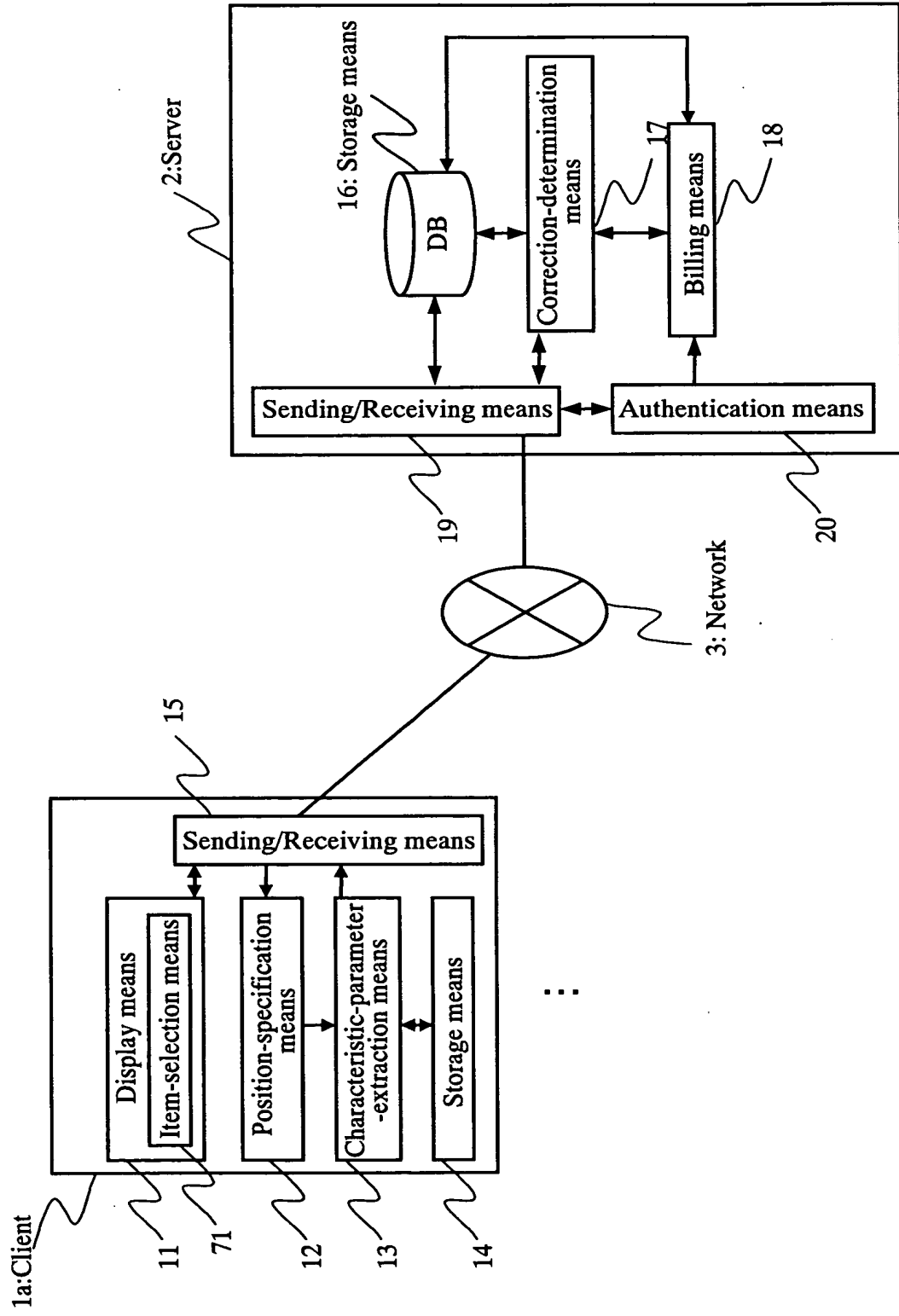




FIG.8

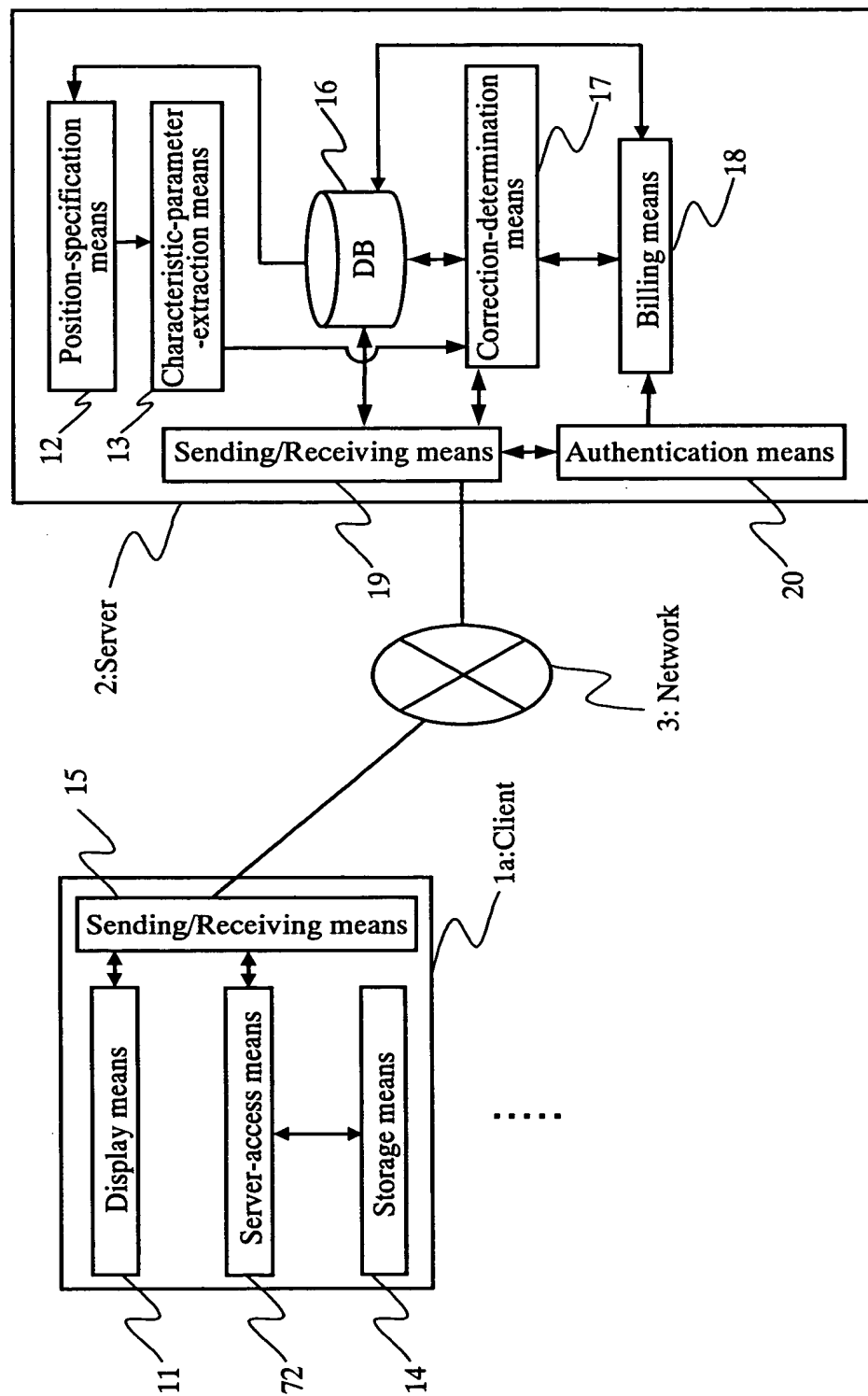


FIG.9

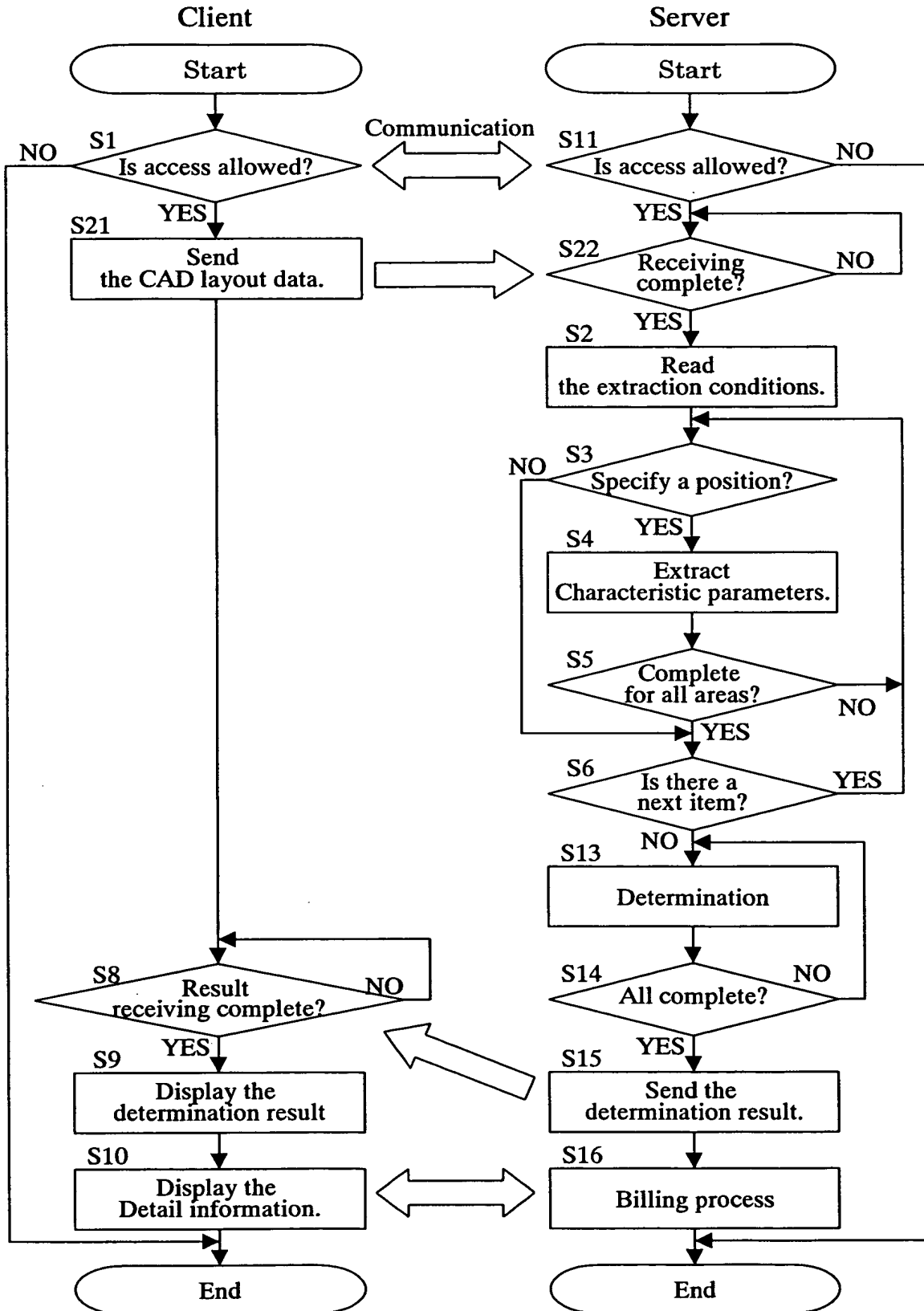


FIG.10

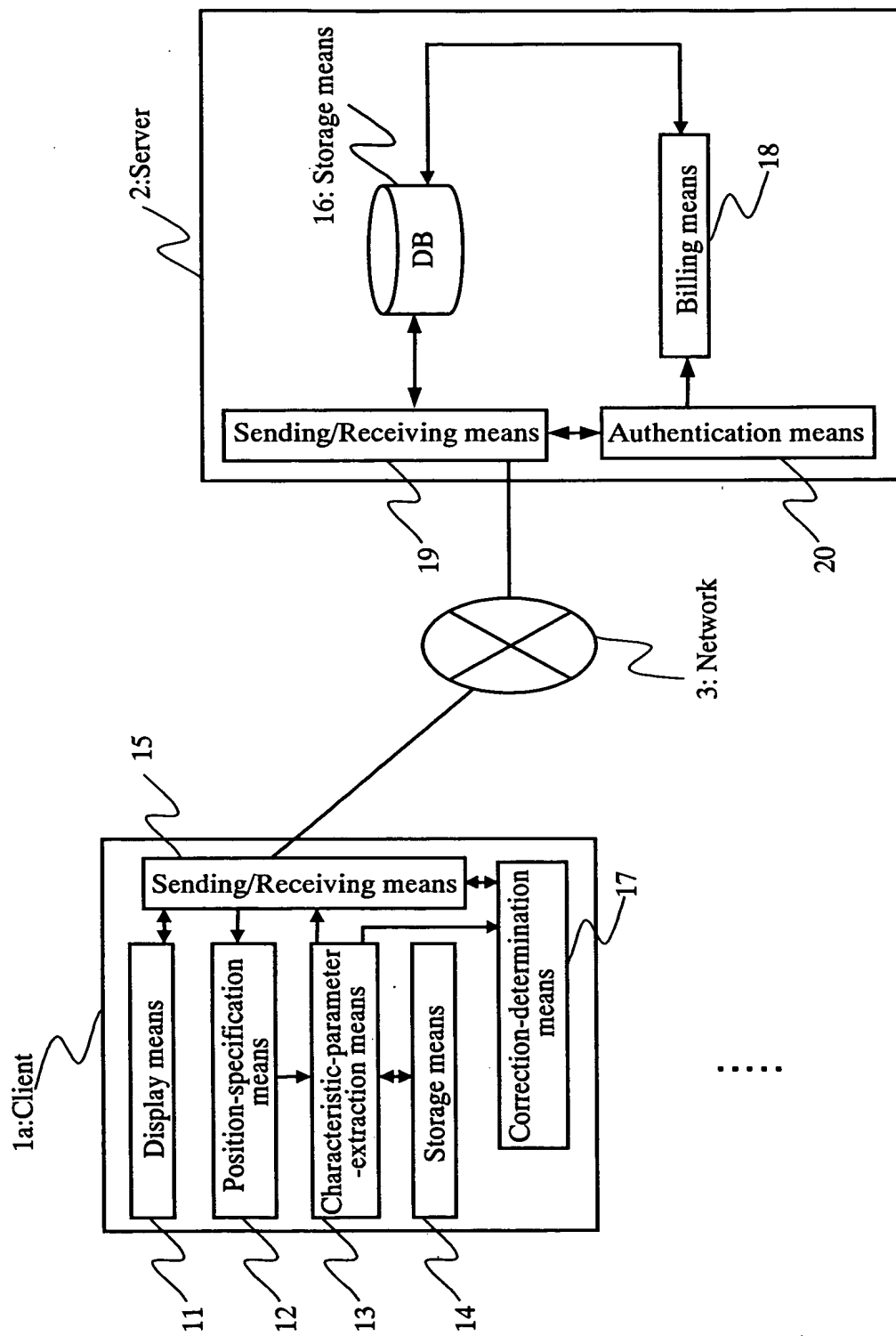


FIG.11

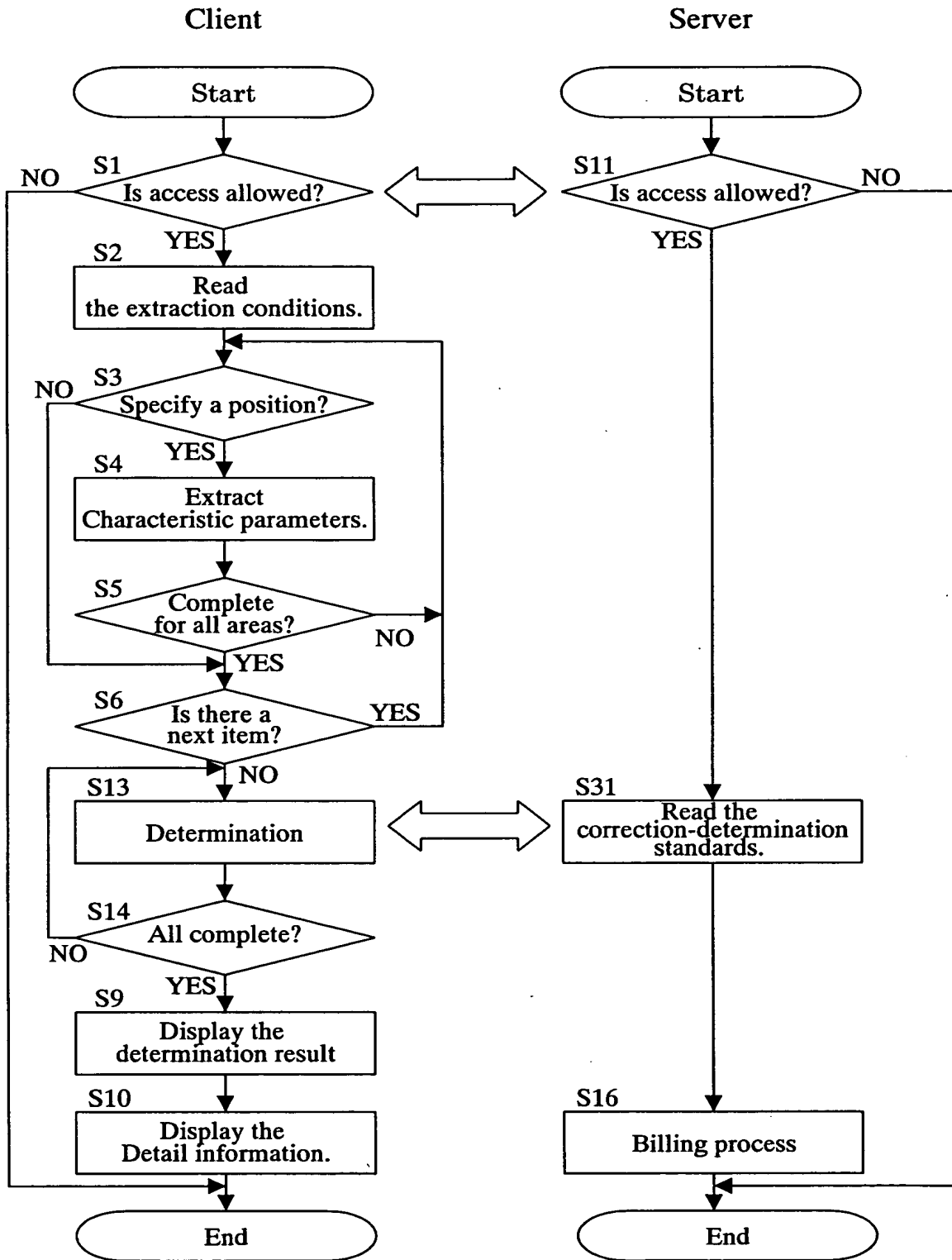


FIG.12

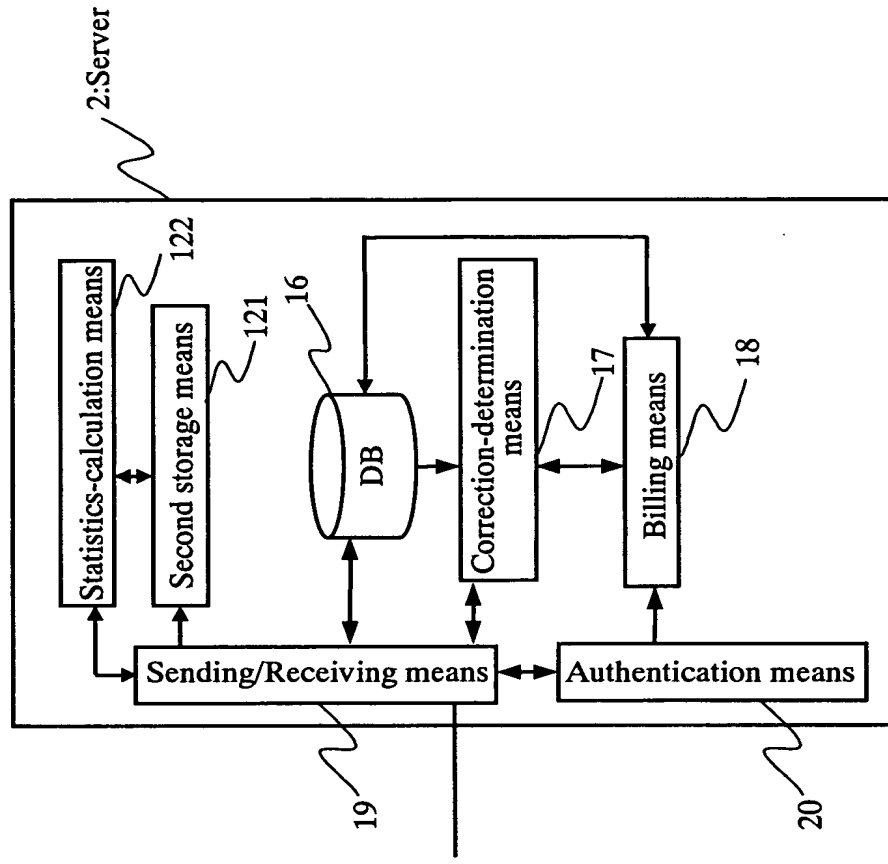


FIG.13

Item number	Number of power-supply pins	Characteristic-parameter items
100	LSI	Number of power-supply pins Number of bypass capacitors
101	LSI	Distance from the LSI power-supply pin to the bypass capacitor
⋮	⋮	⋮

31: Item numbers

32: Position-specification conditions

33: Characteristic-parameter items

FIG.14

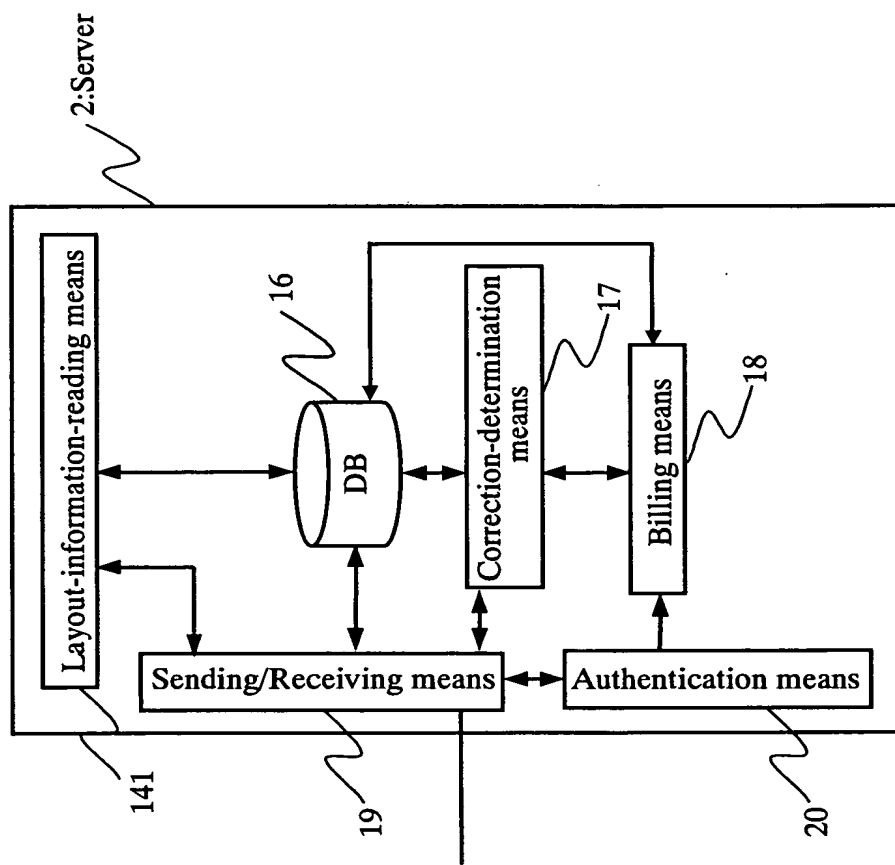


FIG.15

Item number	Position-specification conditions	Characteristic-parameter items
200	Bypass capacitor	Power-supply pin
201	Damping resistor	IC pin to which the clock signal is input
⋮	⋮	⋮

31: Item numbers

32: Position-specification conditions

33: Characteristic-parameter items



FIG.16

Item number	Information related to the CAD layout
200	The bypass capacitor is placed such that the distance to the power-supply pin or distance from the outside to the power-supply-input means is a minimum
201	The damping resistor is placed near the IC pin to which the clock signal is input.
⋮	⋮

31: Item numbers

35: Layout-design information

FIG.17

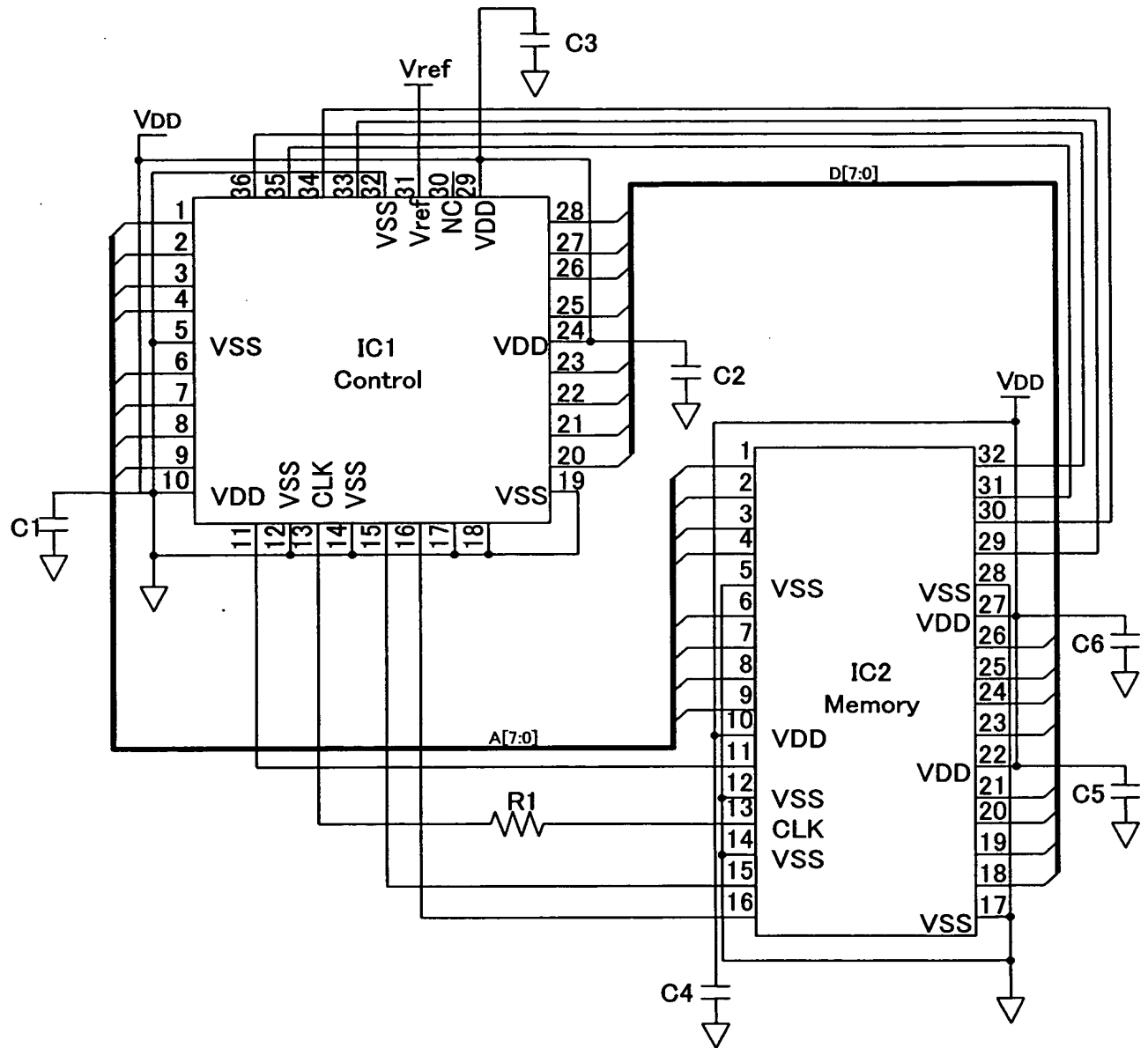
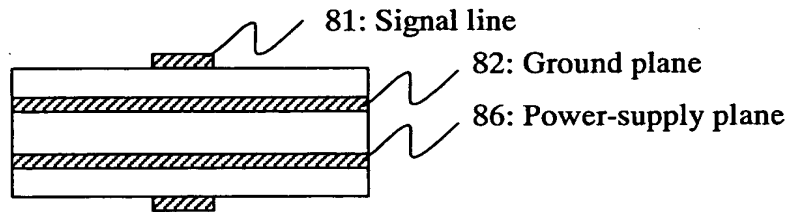


FIG.18

(a) Cross-sectional view



(b) Top view(The insulating layer is omitted.)

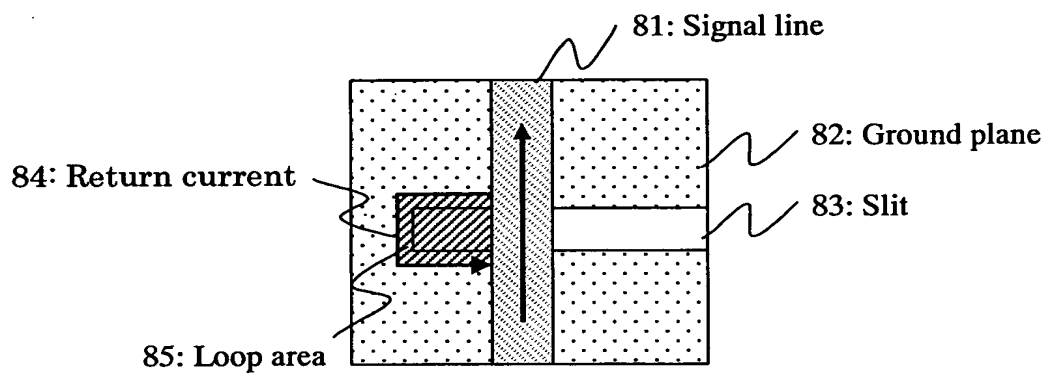


FIG.19

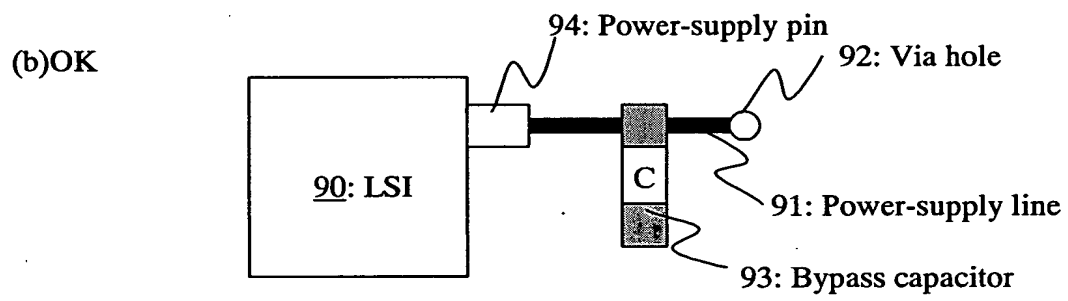
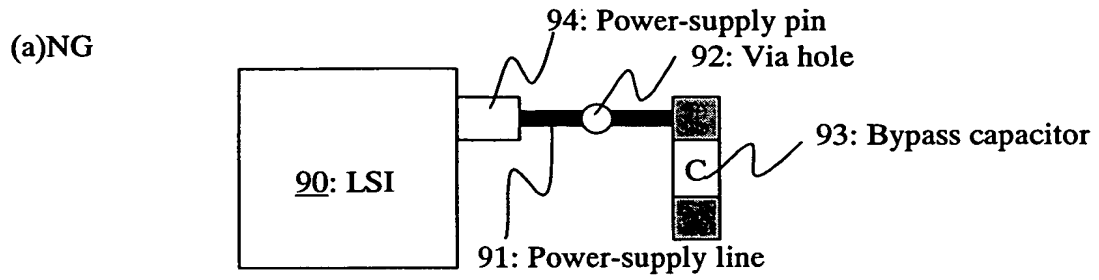
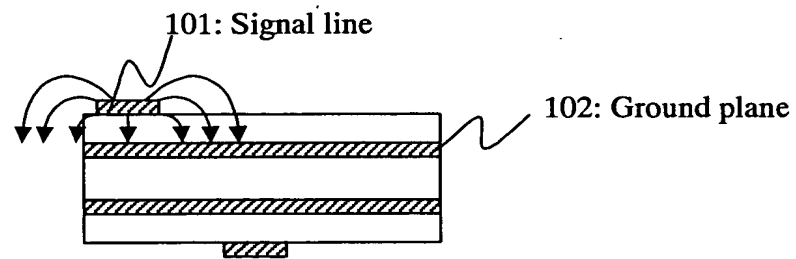


FIG.20

(a) Electric field leakage



(b) No electric field leakage

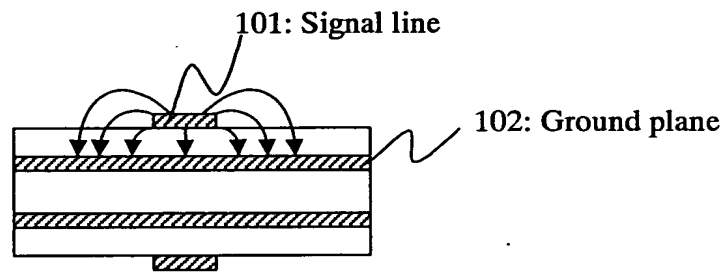
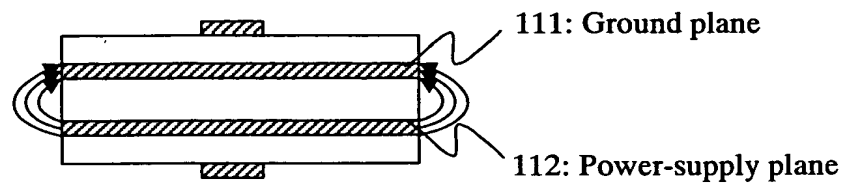


FIG.21

(a) Electric field leakage



(b) No electric field leakage

